

ABSTRACT

A semiconductor device that is capable of suppressing an increase in the chip size while implementing ESD damage countermeasures in which the power supply (or ground) terminal of one power source system serve as the reference potential terminal for the signal terminal of the other power source system is provided. The semiconductor device 1 includes, in first and second power source systems, ESD protective bonding pads 36 to 39 connected by bonding wires 26 to 29 to power supply terminals 10 and 13 and ground terminals 12 and 15, signal ESD protective element sections 41a and 42a that are each connected to the signal bonding pads 31 and 34 and the ESD protective bonding pads 36 to 39 and protect I/O circuits 43 and 44 respectively, and a power source ESD protective element section 40a that is connected to ESD protective bonding pads 36 and 37.